IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

VLSI TECHNOLOGY LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 1:19-cv-977-ADA

PLAINTIFF VLSI TECHNOLOGY LLC'S OPENING CLAIM CONSTRUCTION BRIEF

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[1] All exhibits are attached to the Declaration of Charlotte J. Wen concurrently filed herewith.

I. INTRODUCTION

The claim interpretation process "is simply a way of elaborating the normally terse claim language in order to understand and explain, ***but not to change***, the scope of the claims." *Embrex, Inc. v. Service Eng'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000). Yet time and again, Intel proposes to use this process to rewrite the claims, transforming their scope in ways never contemplated by the inventors and never evaluated by the Patent Office. In many instances, Intel's own proposals make this self-evident; for example, where Intel's "interpretation" repeats the language of a term verbatim and then heaps additional requirements on top of it, Intel is not interpreting the term—it is ***adding*** to it and thus transparently attempting to change its scope.

In other instances, Intel seeks to narrow the claim language by adding verbiage from examples in the patents' specifications, but this is just as improper. It is elementary that the specification cannot enlarge, diminish, or vary the claim language, because "[t]he written description part of the specification itself does not delimit the right to exclude. That is the function and purpose of claims." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir. 1995) (en banc). Intel even argues that one term, "capacitance structure," should be supplanted by examples from preferred embodiments because it is a "means-plus-function" term—even though the term does not include the word "means" and does not include a function.

VLSI's proposed resolutions of the parties' claim construction disputes below focus on the actual claim language, which "frames and ultimately resolves all issues of claim interpretation." *Abtox, Inc. v. Exitron Corp.*, 122 F.3d 1019, 1023 (Fed. Cir. 1997). They are limited in their scope and purpose: to clarify and explain, where needed, the claim terms at bar. And where means-plus-function terms are at issue, the corresponding structures VLSI identifies are—in accord with well-

settled law—limited to those elements clearly linked or associated with, and necessary to perform, the recited function.

II. INTERPRETATION OF MEANS-PLUS-FUNCTION TERMS

A recurring issue here is whether terms at issue are drafted in "means-plus-function" format and, if so, how they should be interpreted. As a threshold matter, to determine whether Section 112 ¶ 6 applies, courts "begin by asking whether the claim limitation employs the word 'means.'" *MTD Prod. Inc. v. Iancu*, 933 F.3d 1336, 1341 (Fed. Cir. 2019). If it does not use the word "means," there is a presumption that the term "conveys sufficiently definite structure and is not subject to § 112, ¶ 6." *Id.* In deciding whether the presumption can be overcome, courts consider among other things "whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015) (en banc).

If a claim element is determined to be a means-plus-function term subject to Section 112 ¶ 6, one must next "identify the function explicitly recited in the claim." *Asyst Techs., Inc. v. Empak, Inc.*, 268 F.3d 1364, 1369 (Fed. Cir. 2001). In doing so, one may not deviate from the language of the claims themselves. *See, e.g.*, *In re Teles AG Informationstechnologien*, 747 F.3d 1357, 1367-68 (Fed. Cir. 2014) ("When construing functional claims under § 112 ¶ 6, '[t]he statute does not permit limitation of a means-plus-function claim by adopting a function different from that explicitly recited in the claim.'").

Next, one "must determine what structure, if any, disclosed in the specification corresponds to the claimed function." *Williamson*, 792 F.3d at 1351. "[S]tructure disclosed in the specification is 'corresponding' structure ***only*** if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Saffran v. Johnson & Johnson*, 712

F.3d 549, 562 (Fed. Cir. 2013) (emphasis in original). "[C]orresponding structure must include all structure that actually performs the recited function," *Cardiac Pacemakers, Inc. v. St. Jude Medical, Inc.*, 296 F.3d 1106, 1119 (Fed. Cir. 2002), including "alternative embodiments of the invention." *Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999). However, the Court "may not import . . . structural limitations from the written description that are unnecessary to perform the claimed function." *Wenger Mfg., Inc. v. Coating Mach. Sys., Inc.*, 239 F.3d 1225, 1233 (Fed. Cir. 2001); *see also Golight, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1334 (Fed. Cir. 2004) (excluding structures "superfluous to our claim construction analysis because they are not required for performing the claimed function"). Details that "more particularly defin[e] the structure in ways unrelated to the recited function" are "not . . . structure ***corresponding*** to the recited function." *Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc.*, 145 F.3d 1303, 1308 (Fed. Cir. 1998) (emphasis in original). "The corresponding structure to a function set forth in a means-plus-function limitation must actually perform the recited function, not merely enable the pertinent structure to operate as intended . . . ." *Asyst*, 268 F.3d at 1371.

Finally, Section 112 ¶ 6 provides that means-plus-function terms include both the corresponding structures described in the specification ***and*** equivalents thereof. 35 U.S.C. § 112 ¶ 6[2]; *Regents of Univ. of Minn. v. AGA Med. Corp.*, 717 F.3d 929, 941 (Fed. Cir. 2013) ("Under section 112 ¶ 6, . . . a means-plus-function claim limitation includes both the corresponding structures disclosed by the specification as means of performing the function, and the equivalents of those structures."); *Callicrate v. Wadsworth Mfg., Inc.*, 427 F.3d 1361, 1369 (Fed. Cir. 2005)

[2] Pre-AIA 35 U.S.C. § 112 ¶ 6 applies because the applications leading to the patents at issue were filed prior to September 16, 2012. *See, e.g.*, *Diebold Nixdorf, Inc. v. Int'l Trade Comm'n*, 899 F.3d 1291, 1296 n.2 (Fed. Cir. 2018).

("Accounting for all structure in the specification corresponding to the claimed function, this term means pivotally mounted cutting mechanisms . . . and, of course, equivalents of these structures.").

III. AGREED CONSTRUCTIONS

The parties agree to the following constructions for U.S. Patent No. 7,606,983:

Claim Term	Agreed Construction
"means for accessing data"	**Function:** "accessing data" **Structure:** "a memory circuit, device or system, or equivalents thereof"
"means for processing series of operations and for generating based thereon access requests for the data"	**Function:** "processing series of operations and generating based thereon access requests for the data" **Structure:** "a processor, or equivalents thereof"
"means for controlling access to the data, for receiving the access requests from each of the processing means, for determining a performance order, and for providing the access requests to the accessing means in the performance order"	**Function:** "controlling access to the data, receiving the access requests from each of the processing means, determining a performance order, and providing the access requests to the accessing means in the performance order" **Structure:** "a memory controller, controller for other shared resources, or equivalents thereof"

IV. DISPUTED CONSTRUCTIONS

A. U.S. Patent No. 6,366,522 ("The '522 Patent")

The '522 Patent, titled "Method and Apparatus for Controlling Power Consumption of an Integrated Circuit," discusses power management features that can "adjust the system clock and/or the supply voltage based on the processing capabilities of an integrated circuit and the application being performed to conserve power." Ex. 1 ('522 Patent), 1:44-47. The patent describes how "power consumption of an integrated circuit can be controlled, and thereby reduced, based on the

application being performed"—allowing for dynamic control of the chip's voltage and frequency that is tailored to the specific program's needs. *Id.*, 2:21-26.

1. "regulate/regulating at least one supply from a power source and an inductance"

VLSI's Proposal	Intel's Proposal
plain and ordinary meaning	"regulate/regulating at least one supply from an inductance connected to a power source, where the inductance is positioned between the power source and the regulating circuitry"

a. This Term Does Not Require Construction

"[A] claim must explicitly recite a term in need of definition before a definition may enter the claim from the written description." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1248 (Fed. Cir. 1998). Here, by repeating every single word that appears in the claim term, including words like "inductance" and "power source," in its proposed construction, Intel admits the relevant words are not "in need of definition." *See, e.g.*, *Biscotti Inc. v. Microsoft Corp.*, 2016 WL 6611487, at *9 (E.D. Tex. Nov. 9, 2016) ("The parties do not appear to dispute that one skilled in the art would not need construction of the term itself as both parties merely repeat the language of the term in their constructions."); *Saint Lawrence Commc'ns LLC v. ZTE Corp.*, 2016 WL 6275390, at *43 (E.D. Tex. Oct. 25, 2016) ("[B]ecause the remainder of Defendants' proposed construction merely repeats the claim language itself, no further construction is necessary."). This term should therefore be given its plain and ordinary meaning. *See, e.g.*, *Va. Panel Corp. v. Mac Panel Co.*, 133 F.3d 860, 866 (Fed. Cir. 1997) ("Without an express intent to impart a novel meaning to claim terms, an inventor's claim terms take on their ordinary meaning.").

b. Intel Seeks To Narrow And Redraft The Claim Language

Intel's construction provides no insight into what it means to "regulate at least one supply from a power source and an inductance." Instead, the construction narrows the term to a specific circuit layout—one where "an inductance [is] connected to a power source . . . [and] positioned between the power source and the regulating circuitry." This improper claim rewriting adds not one, but two, unsupported elements: (i) that the "inductance" be "connected to a power source," and (ii) that "the inductance [be] positioned between the power source and the regulating circuitry." But no discussion in the patent defines this term in such a limited manner. First, nothing in the claim or elsewhere requires that the inductance and power source be "connected." Intel appears to conjure this limitation from thin air. Second, the patent carefully avoids ever committing the inductance to a specific location, first broadly claiming only "an inductance" (*see, e.g.*, Ex. 1, cl. 1), and then specifying in dependent claims that the inductance can be "an external inductance" (*see, e.g.*, Ex. 1, cl. 25). Under long-established law on claim differentiation, this strongly suggests that the original inductance can be either internal or external, and further underscores the lack of any limitations (like Intel's) on its precise location. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (en banc) ("[T]he presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim.").

Intel's proposal also violates black letter law on importing limitations from the specification. The Federal Circuit has made it clear that to limit an otherwise broadly-worded claim, the patentee must make "crystal clear that a particular (*i.e.*, narrow) understanding of a claim term is an 'essential element'" of the invention. *Johnson Worldwide Assocs., Inc. v. Zebco Corp.*, 175 F.3d 985, 993 (Fed. Cir. 1999). Far from a "crystal clear" limiting statement, the patent specification here teaches that, "[a]s one of average skill in the art will appreciate, other

embodiments may be derived from the teachings of the present invention without deviating from the scope of the claims." Ex. 1, 6:50-53. Accordingly, injecting Intel's new limitations would violate the most basic rules of claim construction. As explained in *Phillips*, "if we once begin to include elements not mentioned in the claim, in order to limit such claim . . . we should never know where to stop." 415 F.3d at 1312.

B. U.S. Patent No. 7,292,485 ("The '485 Patent")

Memory cells generally need to be sufficiently stable (operate at high enough voltage) to retain data, but also sufficiently unstable (operate at low enough voltage) to be written onto in the first place. However, some memory cells cannot operate at any single voltage that results in them being stable enough to retain data, and yet unstable enough to be written to, creating an opportunity for optimization. The '485 Patent describes technology that can create short-term instability in memory cells to improve the process of writing data while optimizing the overall stability of the memory cells. For instance, the patent describes a "memory circuit" in which charge is shared with a "capacitance structure" to "provide[] more margin" when writing data into a selected line of memory cells. Ex. 2 ('485 Patent), Abstract.

1. "a capacitance structure"

VLSI's Proposal	Intel's Proposal
plain and ordinary meaning; not means-plus-function	**Function**: providing "capacitance" **Structure**: (1) Dummy column 17 (comprised of dummy SRAM cells 30, 32, and 34 and dummy bitlines SBL and SBL*) and conductor 37, configured to be selectively coupled to one or more of the dummy SRAM cells, as shown in Figure 2; or alternatively (2) dummy row 70 (comprised of dummy SRAM cells 82, 84, and 86 and dummy wordline SWL) and conductor 71, configured to be selectively coupled to one or more dummy of the SRAM cells, as shown in Figure 3

A person of skill in the art would understand the term "capacitance structure" to have its plain and ordinary meaning, which encompasses a well-known class of electronic structures that have capacitance. A person of skill in the art would not conclude that the term "capacitance structure" was intended to invoke Section 112 ¶ 6 for many reasons, including because the term does not use the word "means," because it does not recite a function, and because "the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Williamson*, 792 F.3d at 1349. VLSI's proposal should be adopted for at least these reasons and the others presented below.

First, when a claim term lacks the word "means" there is a presumption that Section 112 ¶ 6 does not apply. *Id.* The claim term here does not include the word "means." Therefore, Intel's construction is presumptively incorrect.

Second, a person of skill in the art would understand that "capacitance" is a physical property, like temperature, mass, or resistance, rather than a function as Intel suggests. Conte

¶ 15.[3] It is not a function. Further corroborating this conclusion is the fact that Intel's proposed function, "providing capacitance," does not appear ***anywhere*** in the '485 Patent or its prosecution history. Instead, the '485 Patent describes certain structures as having "capacitance" or "relative capacitances," *e.g.*, Ex. 2, 4:44-50, 4:64-66; 6:27-30; Conte ¶ 16. Thus, the term Intel contends is "means-plus-function" has neither a means nor a function. Even if the term had included the word "means" (which it does not) and even if "capacitance" could be rewritten as a function (which it should not be), a term may cover "a broad class of structures" and "even . . . identif[y] the structures by their function" without being a means-plus-function term. *Skky, Inc. v. MINDGEEK, S.A.R.L.*, 859 F.3d 1014, 1019 (Fed. Cir. 2017).

Third, a person of skill in the art would understand that the term "capacitance structure" refers to a well-known class of physical structures on an electronic circuit such as capacitors, transistors connected in a manner to have capacitance, and dummy cells having capacitance. Conte ¶ 14. This is another independent reason why this is not a "means-plus-function" term. *See, e.g., Volcano Corp. v. St. Jude Med., Cardiovascular & Ablation Techs. Div., Inc.*, 2014 WL 266155, at *3 (D. Del. Jan. 24, 2014) ("Because 'flexible element' does not contain the word 'means' and the term connotes sufficient structure to a PHOSITA, . . . § 112 ¶ 6 does not apply."); *Katz v. AT & T Corp.*, 63 F. Supp. 2d 583, 600 (E.D. Pa. 1999) (holding that "interface structure" "sufficiently connotes structure such that § 112, ¶ 6 does not apply," because the term "would have called to mind a specific set of structures to a person of ordinary skill in the art such that such a person would be able to build the Katz inventions").

[3] All "Conte" citations refer to the Opening Declaration of Professor Thomas M. Conte, filed concurrently herewith.

Fourth, many of the '485 Patent claims impose additional physical requirements on the claimed "capacitance structure." *E.g.*, Ex. 2, cls. 1, 12 ("capacitance structure includes a plurality of dummy cells"); *id.*, cls. 3, 19 ("capacitance structure comprises: a dummy line; and the plurality of dummy cells coupled to the dummy line"); *id.*, cl. 10 ("capacitance structure comprises a first line and a first plurality of dummy cells coupled to the first line"). *See also, e.g.*, Ex. 6 (Notice of Allowance), 2 (inserting "includes a plurality of dummy cells" after the word "structure" in claims 1 and 12). Intel's proposal, which seeks to include these requirements as part of the base term "capacitance structure," would improperly render these additional structural terms superfluous. *Nautilus Grp., Inc. v. Icon Health & Fitness, Inc.*, 82 F. App'x 691, 694 (Fed. Cir. 2003) (reversing construction that "improperly renders claim terms superfluous"); *Vistan Corp. v. Fadei USA, Inc.*, 2012 WL 1496099, at *20 (N.D. Cal. Apr. 27, 2012) ("Defendants' proposed construction of this term is redundant and renders claim language superfluous.").

Fifth, the claims, the specification, and the prosecution history repeatedly describe how the "capacitance structure" is coupled to and otherwise interacts with other physical structures in the claimed memory circuit. *E.g.*, Ex. 2, cl. 1 ("coupl[ing] the second power supply line to the first capacitance structure"); *id.*, cl. 6 ("a switching transistor coupled between the capacitance structure and a voltage reference terminal"); *id.*, cl. 12 ("transistors that [are] connected between . . . the second power supply line and the first capacitance structure"); Conte ¶¶ 17-21.

Under these circumstances, courts routinely hold that claim elements recite definite structure and, accordingly, that they should not be interpreted as "means-plus-function" elements. *E.g.*, *Powell v. Home Depot U.S.A., Inc.*, 663 F.3d 1221, 1230 (Fed. Cir. 2011) (Section 112 ¶ 6 did not apply to "dust collection structure" because the claim "requires that the 'dust collection structure' and the 'cutting box' be coupled together"); *Black & Decker Corp. v.*

Positec USA Inc., 2013 WL 4839629, at *19, *21 (N.D. Ill. Sept. 10, 2013) (Section 112 ¶ 6 did not apply to "latch receiving structure" because the claim additionally recited that the latch receiving structure included "a ramp portion and latch aperture"); *Coprecitec, S.L. v. Brinkmann Corp.*, 2013 WL 12061898, at *3 (N.D. Ga. Nov. 20, 2013) (construing "rotatable structure" to have its plain and ordinary meaning, because "[t]his language sets forth the physical operation and operation of the parts"). "Capacitance structure," as recited, does not invoke Section 112 ¶ 6, and should be construed in accordance with its plain and ordinary meaning.

2. "precharging means for precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells"

Agreed Function	VLSI's Proposal	Intel's Proposal
"precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells"	**Structure:** "a conductor, or equivalents thereof"	**Structure:** (1) Voltage source V_{REF} and transistor 36, coupled in series to provide a reference voltage to one or more dummy cells through conductor 37, as shown in Figure 2; or alternatively (2) voltage source V_{REF} and transistor 90, coupled in series to provide a reference voltage to one or more dummy cells through conductor 71, as shown in Figure 3

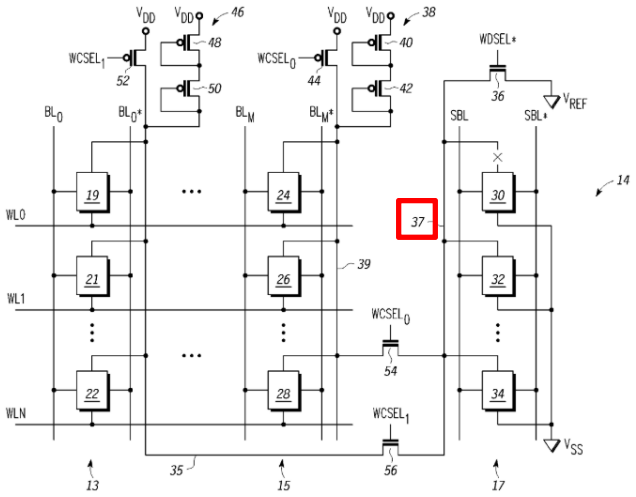
a. "A Conductor, Or Equivalents Thereof" Performs The "Precharging" Function

The '485 Patent discloses that "a conductor," or equivalents thereof, performs the agreed function of "precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells."

The parties appear to agree about the general areas of the specification that describe the structure that performs the "precharging" function, but disagree as to the scope of required

structure. As explained below, only the "conductor," or its equivalents, are necessary. Intel, however, would have the Court add structural limitations that merely enable the conductor to perform the claimed function. But "[i]t is well established that it is not necessary to claim in a patent every device required to enable the invention to be used. . . . The corresponding structure to a function set forth in a means-plus-function limitation must ***actually perform*** the recited function, not ***merely enable*** the pertinent structure to operate as intended." *Asyst*, 268 F.3d at 1371.

The '485 Patent discloses that a "conductor" is the only structure that actually performs the "precharging" function. The patent sets the stage by explaining that: "In operation, prior to writing . . . [r]eference voltage V_{REF} is provided to the supply terminals of each of the memory cells 30, 32, and 34 precharging the cells of dummy column 17 to V_{REF} (ground)." Ex. 2, 4:30-33. A person of skill in the art would understand that "dummy column 17" corresponds to the capacitance structure in this particular embodiment. Figure 2 then illustrates that the conductor (37, label marked with a red box) carries voltage to the capacitance structure, thereby precharging it:



Ex. 2, fig.2; Conte ¶ 25. In another embodiment, the patent states again that: "prior to a write operation, . . . V_{REF} is provided to the supply terminals of each of the memory cells . . . precharging

the cells of dummy row 70 to V_{REF}." Ex. 2, 6:12-16. Figure 3 then also illustrates that conductor 71 carries the voltage to the dummy row (which a person of skill in the art would understand is the capacitance structure in this alternative embodiment). Conte ¶ 26. Thus, a person of skill would understand the ***conductor*** is the ***structure*** that performs the "precharging" function. *See also, e.g.*, Ex. 2 at 4:5-7 ("The amount of capacitance shared is determined in part by how many memory cells are coupled to ***conductor 37***."); Conte ¶ 27.

b. Intel's Proposal Includes Unnecessary Structure

Intel's proposal is improper because it attempts to include elements which at most merely enable, rather than actually perform, the "precharging" function, and also because it attempts to read additional functions and structural limitations into the claim which are inconsistent with the disclosure of the '485 Patent.

First, Intel erroneously contends that, in addition to a conductor, "a voltage source V_{REF} and transistor coupled in series to provide a reference voltage to one or more dummy cells" should be included as corresponding structure. But the transistor merely enables the conductor to perform the precharging function. As explained above, the conductor is the structure which actually carries the reference voltage to the capacitance structure, thereby "precharging" it. Conte ¶¶ 25-27. If one were to include merely enabling structures such as the transistor, one would never know when to stop. Would we also include the wires that supply power to the transistor? Or the internal power supply that energizes those wires? Or the external transmission lines that bring electricity to the power supply? Or the power plant that generates the electricity to begin with? The law clearly directs that merely enabling structures do not qualify as "corresponding" and that law should be followed here.

Second, Intel's proposal improperly attempts to read a "voltage source V_{REF}" into the claim, but the '485 Patent does not discuss a "voltage source." The patent ***does*** discuss a reference voltage

V_{REF}, but a person of skill in the art would understand that a voltage is not a structure at all, let alone a corresponding structure. *E.g.*, *MOSAID Techs. Inc. v. Samsung Elecs. Co.*, 362 F. Supp. 2d 526, 538 n.11 (D.N.J. 2005) ("[T]he Court found that 'clock signals' were voltages, not structure."). And even if V_{REF} could (erroneously) be considered structure, V_{REF} at most ***enables*** the function of precharging the capacitance structure. *Competitive Techs. v. Fujitsu Ltd.*, 286 F. Supp. 2d 1161, 1199-200 (N.D. Cal. 2003) (refusing to include Vcc and ground in corresponding structure because "the connection to Vcc and ground, at most, ***enables*** [the claimed function]"); Conte ¶ 29.

Third, Intel's attempts to include the additional function of "coupl[ing] . . . to provide a reference voltage" in its proposed structure should be rejected. The undisputed function set forth in this claim limitation is "precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells." *Wenger*, 239 F.3d at 1233 ("Under § 112, ¶ 6, a court may not import functional limitations that are not recited in the claim . . . ."); *Micro Chem.*, 194 F.3d at 1258 ("[Section 112 ¶ 6] does not permit limitation of a means-plus-function claim by adopting a function different from that explicitly recited in the claim.").

Fourth, Intel's proposal also attempts to read "dummy cells" into a claim that does not require "dummy cells." As explained above in connection with the "capacitance structure" term, certain claims of the '485 Patent require that the "capacitance structure" include "a plurality of dummy cells," but claims 17-19 (which include the "precharging means" term) do not. Thus, Intel's attempt to read a requirement of "dummy cells" in claim 17 is improper. *SRI Int'l. v. Matsushita Elec. Corp. of Am.*, 775 F.2d 1107, 1122, (Fed. Cir. 1985) (en banc) ("It is settled law that when a patent claim does not contain a certain limitation and another claim does, that limitation cannot be read into the former claim . . . ."). Furthermore, it is the capacitance structure (the "dummy cells" in some embodiments) that are themselves precharged. *See* Conte ¶ 30. The

precharging is performed ***on*** the dummy cells, not ***by*** the dummy cells. Because the dummy cells do not perform the precharging function, they do not qualify as corresponding structure here.

3. "first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" / "second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells"

Agreed Function	VLSI's Proposal	Intel's Proposal
"coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells"	**Structure:** "a switching circuit, or equivalents thereof"	**Structure:** (1) Transistor 52 and clamping circuit 46, configured to couple power supply voltage VDD and conductor 35, as shown in Figure 2 (if the second line of memory cells is SRAM column 15); or alternatively (2) transistor 96 and a clamping circuit, configured to couple power supply voltage
"coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells"	**Structure:** "a switching circuit, or equivalents thereof"	**Structure:** (1) Transistor 54, configured to couple conductor 39 to conductor 37, as shown in Figure 2 (if the second line of memory cells is SRAM column 15); or alternatively (2) transistor 94, configured to couple conductor 69 to conductor 71, as shown in Figure 3 (if the second line of memory cells is SRAM row 68)

a. "A Switching Circuit, Or Equivalents Thereof" Performs The "Coupling" Functions

The '485 Patent links a switching circuit with the functions of "coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" and "coupling the second supply line to the first capacitance structure during the write

operation for the second line of memory cells." *E.g.*, Ex. 2, Abstract ("where the second line of memory cells is selected for writing, ***a switching circuit*** couples the power supply terminal to the first power supply line . . . , and couples the second power supply line to the first capacitance structure"); *id.*, 6:47-58 ("***A switching circuit . . . has transistors that***, when the second line of memory cells is selected for writing, couple the first power supply terminal to the first power supply line, . . . and couple the second power supply line to the first capacitance structure."). Thus, a person of skill in the art would understand that a switching circuit, or equivalents thereof, performs the claimed "coupling" functions. *Saffran*, 712 F.3d at 562 ("structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history ***clearly links or associates*** that structure to the function recited in the claim").

b. Intel's Proposed Structure For The First "Coupling" Function Is Improper

Intel's proposal for the first "coupling" function is improper for at least four independent reasons: (1) it attempts to limit the structure to two exemplary embodiments while disregarding others; (2) it attempts to read limitations into the claims in a manner inconsistent with the patent's disclosure; (3) it attempts to add phrases into the claims that do not appear anywhere in the patent, for any purpose; and (4) its proposed structures do not perform the first "coupling" function, and in fact are affirmatively described by the patent as performing ***other*** functions.

First, Intel's proposed structure excludes multiple exemplary embodiments in favor of focusing solely on Figures 2 and 3 of the patent. Ex. 2, 2:24-26 (introducing fig.1 as just "one embodiment of the present invention"); *id.*, 3:10-11 (fig.2); *id.*, 5:1-2 (fig.3). Intel's approach is improper, because "[a] means-plus-function claim encompasses ***all*** structure in the specification corresponding to that element and equivalent structures"; thus, "[w]hen multiple embodiments in the specification correspond to the claimed function, proper application of § 112, ¶ 6 generally

reads the claim element to embrace each of those embodiments." *Micro Chem.*, 194 F.3d at 1258. Here, Intel ignores embodiments disclosing that VLSI's proposed structure—a "switching circuit," or its equivalents—performs the first "coupling" function. *E.g.*, Ex. 2, Abstract; *id.*, 6:47-58.

Second, Intel improperly attempts to read additional limitations into the claim. For instance, Intel attempts to read an additional function ("coupl[ing] power supply voltage V_{DD} and conductor 35") into the claim. But "power supply voltage V_{DD}" and "conductor 35" are not corresponding structure because they generally correspond to the elements ***being coupled*** by the function as opposed to the elements that themselves perform the coupling. Intel's inclusion of reference numerals is also improper because they are not limiting. *See* MPEP § 608.01(m) ("The use of reference characters is to be considered as having no effect on the scope of the claims."); *Core Wireless Licensing S.A.R.L. v. LG Elecs., Inc.*, 2015 WL 6956722, at *7 (E.D. Tex. Nov. 9, 2015) ("[T]he rationale for excluding [reference] numbers is equally applicable to means-plus-function terms. The Court finds that the function does not include the reference numbers.")

Third, Intel mischaracterizes the specification. The phrases "transistor 52 and clamping circuit 46, configured to couple power supply voltage V_{DD} and conductor 35" and "transistor 96 and a clamping circuit, configured to couple power supply voltage V_{DD} and conductor 67," do not appear anywhere in the '485 Patent. Indeed, the patent does not mention anything being "configured to" perform any function, let alone the first "coupling" function.

Fourth, Intel's proposed structures simply do not perform the function of "coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells." Indeed, the patent explicitly states that Intel's proposed "transistors" and "clamping circuits" serve entirely different functions during the write operation. With respect to transistors 52 and 96, the '485 Patent states that these transistors ***are decoupled*** during a write

operation: "During a write operation, . . . decoded control signals . . . are asserted . . . to cause transistors 52 and 44 to ***be substantially non-conductive***." Ex. 2, 4:33-36; *id.*, 6:16-19 (same for "transistors 96 and 98"). Thus, a person of skill in the art would understand that these transistors do not "coupl[e] the power supply terminal to the first power supply line during the write operation." Conte Decl. ¶ 35. With respect to the clamping circuits, the '485 Patent specification does not associate any "clamping circuit" with the first "coupling" function. Instead, the specification explicitly states that, during the write operation, the "clamping circuits ***function to limit the voltage drop*** on conductors 67 and 69." Ex. 2 at 6:31-32; *id.* at 4:50-52 ("clamping circuits 38 and 46 function to limit the voltage drop on conductors 35 and 39"); *see also* Conte Decl. ¶ 36.

In other words, neither of Intel's proposed structures perform the first "coupling" function—to the contrary, they serve other, unrelated purposes. Thus, they are not "corresponding structure" for the first "coupling" function, and the Court should adopt VLSI's proposed structure of "a switching circuit, or equivalents thereof." *See, e.g.*, *Koninklijke Philips N.V. v. Zoll Lifecor Corp.*, 2016 WL 6917268, at *6 (W.D. Pa. Mar. 2, 2016) ("Thus, 'current sensor' 68 is not 'clearly linked' to the claimed function, performs a different function, and is not properly part of the 'corresponding structure.'").

c. Intel's Proposed Structure For The Second "Coupling" Function Is Unduly Restrictive

Intel's proposed structure for the second "coupling" function similarly fails.

First, Intel again attempts to limit corresponding structure to only two exemplary embodiments while disregarding many others. As explained in further detail above, "corresponding structure" for a means-plus-function claim cannot exclude embodiments disclosed in the patent, and the '485 Patent clearly discloses that ***multiple different structures*** perform the

second "coupling" function, including a "switching circuit," Ex. 2, Abstract, and a "switching circuit with transistors," *id.*, 6:47-58. The patent does arguably disclose two of these "transistors" as examples of equivalent structures that perform the second "coupling" function. However, the '485 Patent ***also*** discloses that the two transistors (given reference numbers 54 and 94) "can be different"—*i.e.*, replaced with different transistors or combinations of transistors:

> In other embodiments, transistors 54 and 56 ***can be different***. For example P-channel transistors can be used, or a combination of P-channel and N-channel transistors can be used. . . .
>
> In other embodiments, transistors 92 and 94 ***can be different***. For example P-channel transistors can be used, or a combination of P-channel and N-channel transistors can be used.

Ex. 2, 4:20-23, 6:3-6. Thus, Intel's proposed construction is too limiting and erroneously excludes multiple embodiments disclosed in the specification.

Second, here again, Intel's proposal improperly attempts to read additional limitations, which are inconsistent with the patent, into the claim. As with the first "coupling" function, Intel attempts to read an additional function (here, "coupl[ing] conductor 39 to conductor 37") into the construction for structure, and again improperly attempts to limit the scope of the claim through the inclusion of reference numbers. *Core Wireless Licensing*, 2015 WL 6956722, at *7.

Thus, Intel's proposed structure should be rejected, and the Court should adopt VLSI's proposed structure of "a switching circuit, or equivalents thereof."

4. "decoupling means for decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells"

Agreed Function	VLSI's Proposal	Intel's Proposal
"decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells"	**Structure:** "a switching circuit, or equivalents thereof"	**Structure:** None, indefinite

The '485 Patent explicitly discloses that a switching circuit, or equivalents thereof, perform the recited function of "decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells." For example, the patent states that: "where the second line of memory cells is selected for writing, ***a switching circuit*** . . . decouples the first power supply line from the second line of memory cells . . . ." Ex. 2, Abstract. In another passage, the patent similarly states: "***A switching circuit … has transistors that***, when the second line of memory cells is selected for writing . . . decouple the first power terminal from the second line of memory cells."). Ex. 2, 6:47-58. Thus, a person of skill in the art would understand that a switching circuit, or equivalents thereof, perform the claimed "decoupling" function. *See* Conte ¶¶ 39-42.

The Federal Circuit instructs that "a challenge to a claim containing a means-plus-function limitation as lacking structural support requires a finding, by ***clear and convincing evidence***, that the specification lacks disclosure of structure sufficient to be understood by one skilled in the art as being adequate to perform the recited function." *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1376-77 (Fed. Cir. 2001). The evidence here shows the opposite; the patent clearly teaches (in multiple locations) that a switching circuit performs the recited function.

C. U.S. Patent No. 7,523,373 ("The '373 Patent")

The '373 Patent describes approaches that, among their other applications, allow a processor to slow down during periods of low activity—and thus conserve power—without losing the information stored in its local memory. In other words, portions of an integrated circuit can scale to voltages lower than what some of the integrated circuit's memory systems could support for certain operations. As one example, the patent describes a manner of providing a minimum operating voltage to a memory even when a dynamic voltage and frequency state selected by the processor calls for a voltage that is lower than that minimum operating voltage.

1. "means for providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage"

VLSI's Proposal	Intel's Proposal
Function: "providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage" **Structure:** "power supply selector, charge pump, scalable voltage regulator, or equivalents thereof"	Indefinite

Because this limitation recites a "means" for performing a function, there is a presumption that it is a means-plus-function limitation within the scope of Section 112 ¶ 6. *E.g.*, *Greenberg v. Ethicon Endo-Surgery, Inc.*, 91 F.3d 1580, 1584 (Fed. Cir. 1996). The recited function is "providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage." No further construction of the recited function is needed.

Intel's indefiniteness argument—whatever it might be—has been waived. Intel failed to disclose any such argument in its preliminary invalidity contentions or any update thereto, despite making indefiniteness arguments therein about other terms in this patent. *See* Ex. 10 (Intel's Preliminary Invalidity Contentions), 794-795.

Even if Intel had preserved its ability to argue that this term was indefinite, which it did not, it would have needed to prove that defense by clear and convincing evidence. *See, e.g.*, *Budde*, 250 F.3d at 1376-77. But as shown below, the specification clearly links each of ***three*** separate structures to the recited function. This term is anything but "indefinite."

a. Power Supply Selector

(1) The Power Supply Selector Can Provide The Memory's Operating Voltage

The patent describes embodiments in which a power supply selector performs the recited function. In these embodiments, the selector can provide the operating voltage to the memory. To do so, it selects among multiple voltages available to it to ensure that the voltage it provides to the memory is at least as great as the memory's minimum operating voltage—including in response to the processor selecting an operating value that is below that minimum voltage.

For example, as shown in the example embodiment of Figure 1 (reproduced below), the patent describes a system that uses two voltage regulators to supply two voltages for the embodiment, VDDmem and VDDlogic. Both voltages are provided to a power supply selector, which, as seen in Figure 1, in turn provides a voltage level to memory array 22. The power supply selector "selects one of VDDmem and VDDlogic based on information provided by controller 28 via, for example, the memory control signals." Ex. 3 ('373 Patent), 2:55-57. Thus, the '373 Patent teaches that a power supply selector "receives VDDmem and VDDlogic and ***provides*** one of these to [a memory] as the memory operating voltage." Ex. 3, 2:52:55. Thus, one structure clearly

linked with "providing" voltage to the memory is the power supply selector, which selects between VDDlogic and VDDmem and provides one of these voltages to a memory.

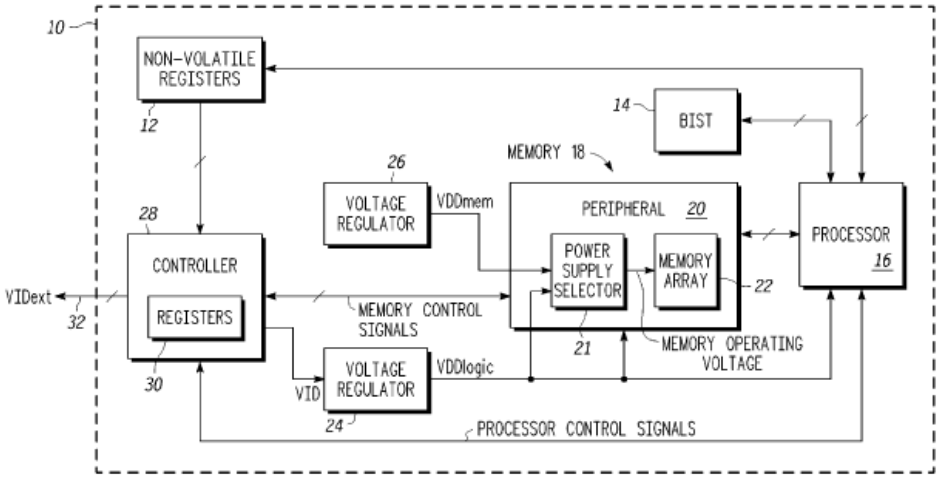


FIG. 1

(2) The Power Supply Selector Can Provide The Voltage At A Value At Least As Great As The Memory's Minimum Operating Voltage

One of the power selector's jobs in these embodiments is to ensure that the voltage provided to the memory is at least as great as the memory's minimum operating voltage.

For example, the patent teaches that VDDlogic can scale, Ex. 3, 3:4-8, and further that it may scale below the minimum operating voltage of the memory. When it does so, the power supply selector can switch to another voltage (such as VDDmem), to provide a voltage to the memory at least as great as its minimum operating voltage. For example,

> while VDDlogic remains above a minimum operating voltage required for successful reads of memory array 22, power supply selector 21 selects VDDlogic as the memory operating voltage provided to memory array 22, such that the memory operating voltage is substantially equal to VDDlogic. When VDDlogic is scaled to a voltage that is below the minimum memory operating voltage required for reads, power supply selector 21 selects the higher voltage, VDDmem, during read cycles to ensure that reads can still be successfully performed.

Id., 3:30-39. Here, one having ordinary skill in the art would understand that reading memory is one way of operating it—for example, the patent explains that "[w]hen VDDlogic is scaled to a voltage that is below the minimum memory operating voltage required for reads, power supply selector 21 selects the higher voltage . . . to ensure that reads can still be successfully performed." *E.g.*, Ex. 3, 3:34-38. Thus, a voltage that "ensure[s] that reads can . . . be successfully completed" in the passage above (*i.e.*, VDDmem) is at least as great as a minimum operating voltage.

As another example, the patent discloses that a memory can have "one or more minimum operating voltages" such as "minimum VDDlogic read voltages," Ex. 3, 6:22-25, which the patent specifically teaches "indicate ***the minimum VDDlogic voltage where [a memory array] can perform reads using VDDlogic*** rather than VDDmem." *Id.*, 4:13-16; *see also, e.g.*, *id.*, 4:6-45 (describing minimum operating voltages); *id.*, 5:16-41. In other words, VDDlogic is used when it is above the minimum operating voltage, such as a minimum read voltage; and when VDDlogic scales below that level, the power supply selector can instead provide the memory with VDDmem, which is at least as great as the minimum operating voltage.

In yet another example,

> controller 28 indicates to power supply selector 21 which power supply to select, VDDmem or VDDlogic (or, if available, VDDmem-write), by monitoring the VDDlogic VID selected within controller 28 . . . and corresponds to the desired value for VDDlogic, and determining when the VDDlogic VID indicates a voltage that is below any of the minimum VDD logic voltages described above.

Ex. 3, 5:41-48. Here, too, the patent teaches that VDDlogic may scale below a minimum operating voltage of the memory, and that a preferred course of action in that event is to provide to the memory another voltage, such as VDDmem or VDDmem-write, which is at least as great as the minimum operating voltage.

(3) The Power Supply Selector Can Provide That Voltage In Response To The Operating Value Selected By The Processor Being Below The Minimum Operating Voltage

The patent teaches that one of the reasons why the power supply selector would provide VDDmem to the memory in some preferred embodiments is in response to the processor selecting a value for VDDlogic that is lower than the memory's minimum operating voltage.

In particular, the patent teaches that the processor can be responsible for scaling VDDlogic by selecting DVFS states (each of which is associated with a VDDlogic voltage level) with the controller: "Controller 28 may provide a selected state signal to select a DVFS state (where controller 28 may provide this signal ***based on a state selected by processor 16***)." Ex. 3, 8:21-23. The state selected by the processor corresponds with an "encoded . . . voltage," *id.*, 8:18-19, which refers specifically to the value of VDDlogic. *See, e.g.*, *id.*, 8:31-33 ("For example, the selected voltage state corresponds to the desired voltage value for VDDlogic."). One having ordinary skill in the art would understand that the "operating value" selected by the processor could in an implementation correspond to an operating frequency; for example, the patent states that the terms "value" or "voltage" can sometimes be used interchangeably depending on context. *E.g.*, *id.*, 6:33-36 ("[M]emory 18 is tested to determine the minimum operating voltages and these voltages ***or values*** representative of these voltages are then stored . . . ."); *id.*, 5:46 ("desired value for VDDlogic"); *id.*, 8:31-33, 22-23 ("[T]he selected voltage state corresponds to the desired voltage value for VDDlogic," and is selected by the processor); *see also, e.g.*, *id.*, 9:14-22.

In other words, the power supply selector in some of the embodiments can provide VDDlogic to the memory so long as VDDlogic is at least as great as the minimum operating voltage of the memory. When the processor selects a value of VDDlogic that is below the minimum operating voltage, power supply selector can instead provide VDDmem—which is selected to be at least as great as the minimum operating voltage of the memory.

b. Scalable Voltage Regulator

The patent also teaches that a scalable voltage regulator may correspond to the recited function. For example, in one embodiment, the controller includes a comparator and override circuit. Ex. 3, 8:16-37. If the processor selects a dynamic voltage frequency state wherein "the desired voltage value for VDDlogic . . . . is below second minimum read voltage 37 or minimum write voltage 38, ... comparator and override 44 may force a different voltage selection that remains above the appropriate minimum voltage." *Id.*, 8:33-42. In these circumstances "controller 28 may adjust VID accordingly to prevent [scalable voltage] regulator 24 from outputting the desired voltage selected by the selected state signal." *Id.*, 8:42-44. In other words, the scalable voltage regulator provides the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage.

c. Charge Pump

Similarly, the patent teaches that "when VDDlogic is to fall below the first minimum operating voltage, ... VDDlogic may be boosted during reads through the use of a charge pump, where this boosted VDDlogic is provided to memory array 22 for reads." *Id.*, 5:54-61.

Accordingly, the function of "providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage" as recited in Claim 13 corresponds to a power supply selector, a charge pump, a scalable voltage regulator, or equivalents thereof.

D. U.S. Patent No. 7,606,983 ("The '983 Patent")

The '983 Patent describes a protocol for communicating between multiple electronic systems. The protocol can specify, among other things, how the communications may be ordered relative to each other. The protocol allows reordering of communications in a manner that

improves performance while avoiding errors that might otherwise be introduced by the reordering. The technology is useful for purposes such as optimizing the efficiency with which digital systems having multiple functional modules (such as processors) are able to make requests of shared resources (such as memory). Ex. 4 ('983 Patent), 1:8-22.

1. "an indication of a/the specified order"

VLSI's Proposal	Intel's Proposal
plain and ordinary meaning	"a second, different indication that indicates a/the specified order"

The parties do not dispute this term's plain and ordinary meaning. For example, Intel's proposed construction does not address any of the arguably technical portions of this term, such as "indication" or "specified order," and instead reuses these words verbatim, assuming—correctly—that they can be understood without further explanation. The kind of construction that Intel seeks is inappropriate in these circumstances. *See, e.g.*, *Biscotti Inc. v. Microsoft Corp.*, 2016 WL 6611487, at *9 (E.D. Tex. Nov. 9, 2016) ("[O]ne skilled in the art would not need construction of the term itself as both parties merely repeat the language of the term in their constructions.").

The disagreement between the parties is limited to Intel's suggestion that the Court append extra-textual constraints onto the term by narrowing the recited "indication" to both a "second" and "different" indication. There is no basis to add such new limitations. Moreover, these limitations appear designed to exclude—erroneously—numerous preferred embodiments. This term should accordingly be left to its undisputed plain and ordinary meaning.

The patent nowhere requires the indication recited in this claim term to be "second" or "different" from any other indication. To the contrary, the patent describes numerous preferred embodiments that intermingle the two recited indications within a single data field. Intel's

proposed construction—with its extra-textual "second" and "different" limitations—could confuse a fact-finder into concluding that embodiments of this sort fall outside the scope of the claims.

For example, in a section of the specification titled "Best Mode For Carrying Out The Invention," the inventors disclose a series of embodiments that use so-called "transaction-ordering signals." Ex. 4, 5:65-7:22. In these embodiments, the transaction-ordering signals "are the mechanism by which requestor 110 indicates to responder 140 whether each occurrence of a request is to be performed in an ordered manner or in an unordered manner, and, if ordered, what the ordering constraint on that request is." *Id.*, 6:28-32. The patent teaches that the "transaction-ordering signals include thread ID signals 370, sequence number signals 372 and last in thread signal 374." *Id.*, 6:26-28. And "[***a***]***ny two*** of thread ID signals 370, sequence number signals 372 or last in thread signal 374 may be ***omitted***." *Id.*, 6:35-37.

Thus, a preferred embodiment can opt to "indicate[] to responder 140 whether each occurrence of a request is to be performed in an ordered manner or in an unordered manner, and, if ordered, what the ordering constraint on that request is" using ***only*** the thread ID signals, ***only*** the sequence number signals, or ***only*** the last in thread signal.

In these embodiments that use only ***one*** of the array of disclosed transaction-ordering signals, the single transaction-ordering signal may provide both indications. For instance, the specification explains that "[i]f thread ID signal 370 is the only transaction-ordering signal used, then a value of zero indicates an unordered transaction." *Id.*, 6:38-40. But if thread ID signal is ***not*** zero, that non-zero value can then function as the claimed indication of "the specified order." *Id.*, 6:40-47. A similar analysis applies to embodiments where "sequence-number signal 372 is the only transaction ordering signal used": a zero is used to indicate an "unordered" transaction, and non-zero values are used as an indication of the specified order. *Id.*, 6:64-7:7.

Intel's demand for a "second" and "different" indication could exclude those preferred embodiments from the scope of all of the patent's claims. But a "construction that excludes a preferred embodiment is rarely, if ever, correct." *C.R. Bard v. U.S. Surgical Corp.*, 388 F.3d 858, 865 (Fed. Cir. 2004).

Because there is no basis for Intel's proposed requirements and the artificial narrowing of claim scope that may follow, Intel's proposed construction should be rejected. This claim term should be left to its plain and ordinary meaning, which neither party contends requires clarification.

E. U.S. Patent No. 7,793,025 ("The '025 Patent")

The '025 Patent relates generally to technology capable of handling external signals called "interrupt requests" in an optimized manner based on system mode. In some embodiments, the technology improves performance by routing interrupt requests to the cores best-suited to handling them at a given point in time, and can take into account that some cores are in reduced power or sleep states at certain junctures.

1. "priority level information associated with a [first/second] system mode for each of the one or more interrupt requests" / "priority level information associated with a [first/second] system mode"

Claim Term	VLSI's Proposal	Intel's Proposal
"priority level information associated with a [first/second] system mode for each of the one or more interrupt requests"	plain and ordinary meaning	"priority level information associated with a [first/second] system mode for each of the one or more potential interrupt requests"
"priority level information associated with a [first/second] system mode"	plain and ordinary meaning	"priority level information associated with a [first/second] system mode for each of the one or more potential interrupt requests"

The '025 Patent describes methods and systems that optimize the performance of computer systems using a type of signal called "interrupt requests." The methods and systems at some times,

and in some places, operate on actual, pending interrupt requests—*e.g.*, requests that have been received in the processor but have not yet been acted upon by interrupting program execution. *See* Ex. 5, 2:61-63 ("Results of the logical combination operation specify one or more enabled, pending interrupt requests, which may be stored in an interrupt pending register."); *id.*, 3:7-12; *id.*, 10:2-6; *id.*, 10:15-21; Conte ¶ 45.d. At other times or places, the patent also discusses "potential" interrupt requests—*e.g.*, possible future requests that have not yet been issued, but might be issued at some later point. *E.g.*, Ex. 5, 2:54-57 ("For example, an interrupt enable register stores masking bits corresponding to each of the potential interrupt requests…."), *id.*, 2:57-61; Conte ¶ 45.a. The patent also discusses three other types of interrupt requests: masked interrupt requests (*e.g.*, requests that have been received by the processor but will not be acted upon), received interrupt requests (*e.g.*, requests that have reached the processor), and handled interrupt request (*e.g.*, requests that have been received and acted upon by interrupting program execution and executing an interrupt handler). *Id.* ¶ 45.b-c, e. Thus, the patent plainly differentiates, both in terms of language and functionality, among at least five different types of interrupt requests. These distinctions are not limited to the specification, but carry over to the claims. For example, claim 1calls for "interrupt requests," while claims 17 and 20 call for a "potential pending interrupt request."

Intel attempts to undo this distinction by changing the plain language of the claims. In particular, Intel seeks to rewrite claim elements calling for "interrupt requests" so that they would be limited exclusively to "potential interrupt requests." Intel also seeks to rewrite claim 9 with the additional verbiage: "for each of the one or more potential interrupt requests."

This is improper. Intel is not trying to interpret anything. To the contrary, Intel retains the full, original language of the claim—but then for claim 1 adds a new, extraneous limitation on top

of it. Worse yet, for claim 9, Intel adds an entire extraneous phrase. "[I]nterpreting what is ***meant*** by a word in a claim 'is not to be confused with adding an extraneous limitation … which is improper.' … [T]he claims as allowed are what we have to deal with and it is not for the courts to say that they contain limitations which are not in them." *Intervet Am., Inc. v. Kee-Vet Labs., Inc.*, 887 F.2d 1050, 1053-54 (Fed. Cir. 1989); *see also Effective Expl., LLC v. Bluestone Nat. Res. II, LLC*, 2017 WL 3193322, at *15 (E.D. Tex. July 27, 2017) (rejecting defendants' construction because it "simply uses the exact language of the claim, but adds the word 'separate' to it").

What Intel is proposing is claim narrowing, not claim interpretation. "[T]here are at least five different types of interrupt requests discussed in the patent and cited art" and a person of ordinary skill in the art "would not understand the general term 'interrupt' in the claims to be narrowly restricted to only 'potential' interrupts." Conte ¶¶ 46-47. "Claim construction should not be a backdoor process by which the scope of a claim is narrowed or expanded, thereby altering the scope of the invention with respect to which the patentee has exclusion rights." *Famosa, Corp. v. Gaiam, Inc.*, 2012 WL 865687, at *2 (S.D.N.Y. Mar. 14, 2012).

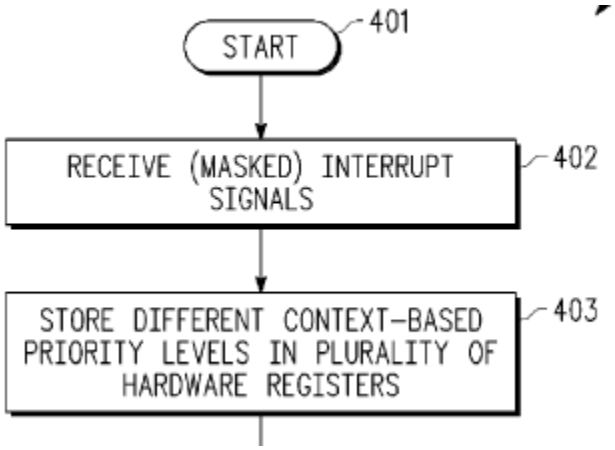
Intel's proposal is all the more inappropriate because the term "potential" appears explicitly in claims 17 and 20, yet is absent from claims 1 and 9. The inventors' decision to direct each of those claims to different subject matter should be respected. Had the inventors wanted to limit claims 1 and 9 to "potential" requests, they plainly could have done so. They did not. *See Unwired Planet, LLC v. Apple Inc.*, 829 F.3d 1353, 1359 (Fed. Cir. 2016) (explaining that a limitation in a non-asserted claim should not restrict the claims-at-issue, and noting that if the patentee intended such restriction, "it could have included that same limitation").

The patent's prosecution history similarly underscores that the inventors did not intend for "potential" to be added to claims 1 and 9. For example, the inventors explained in pertinent part:

> [T]he cited art fails to disclose or suggest Applicants' disclosed interrupt handling methodology which stores priority level information "for each of the one or more interrupt requests" (claim 1) ***or*** "each potential pending interrupt request" (claim 17) in different "interrupt priority storage devices," depending on which system mode is implicated. . . .
>
> Claim 17 likewise differs from [prior art reference] Kershaw in specifying that each stored set of priority levels 'specifies a priority level for each potential pending interrupt request.

Ex. 7 (Applicant's Remarks), 7, 9. All of these statements confirm that the inventors chose to recite "potential" in claim 17 (and claim 20), but not in claims 1 and 9.

Intel seemingly seeks to narrow the claims in an effort to exclude embodiments having interrupt requests that have been made but not yet received, as well as embodiments having interrupt requests that have been received. But this would exclude numerous preferred embodiments. For example, Figure 4 shows an embodiment in which interrupt signals are received:



Ex. 5, fig.4. In this example flow diagram, "the data processing system is activated or already operating." *Id.*, 9:18-19. "A first storage device (e.g., an interrupt source register or interrupt pending register) having a plurality of inputs is provided, where each of the inputs is coupled to receive and store one or more interrupt requests from an interrupt source." *Id.*, 9:19-23. After the system has received one or more interrupt requests, at step 402, the system stores different context-

based priority levels in a plurality of hardware registers. *Id.*, fig.4; *see also id.*, 9:24-33. "[A] construction that excludes a preferred embodiment is rarely, if ever, correct." *C.R. Bard*, 388 F.3d at 865; *see also* Conte ¶ 47.

Intel's attempted revisions are unnecessary. They are inconsistent with the language of the terms at issue, contrary to other claims of the patent, and contrary to preferred embodiments. They seek to significantly narrow, not interpret, the terms at issue. They should be rejected.

2. "storage device for storing priority level information" / "sets of priority levels in … storage devices"

Claim Term	VLSI's Proposal	Intel's Proposal
"storage device for storing priority level information"	plain and ordinary meaning	"hardware for storing priority level information that is not rewritten by software when the system changes mode or context"
"sets of priority levels in … storage devices"	plain and ordinary meaning	"hardware for storing priority levels that are not rewritten by software when the system changes mode or context"

VLSI does not object to providing that a storage device is hardware for storing information, although that does not seem necessary. The remainder of Intel's proposal, however, is yet another effort to append new elements onto a term that does not contain them, as opposed to interpreting words that are actually part of the term. That is improper. *See, e.g.*, *Biscotti*, 2016 WL 6611487, at *9 ("The term 'set-top box video stream' in itself does not mandate [defendant]'s proposed additional limitations. The parties do not appear to dispute that one skilled in the art would not need construction of the term itself as both parties merely repeat the language of the term in their constructions."); Conte ¶ 49 ("A person of skill in the art would not interpret the claims by adding new requirements to them regarding [how priority level information is "rewritten" when the system changes mode or context].").

In particular, Intel seeks to narrow claims 1, 9, and 17 so that priority level information and priority levels are "not rewritten by software when the system changes mode or context." Nothing in the terms even remotely suggests this, let alone requires it. Intel is attempting to narrow the claims by importing elements into them from selected embodiments in the specification. That is fundamentally inappropriate. *Kara Tech. Inc. v. Stamps.com Inc.*, 582 F.3d 1341, 1348 (Fed. Cir. 2009) ("The patentee is entitled to the full scope of his claims, and [the Court must] not limit him to his preferred embodiment or import a limitation from the specification into the claims.").

Worse yet, Intel's proposal to limit the claims to particular preferred embodiments would exclude other preferred embodiments. For example, the detailed description provides: "By implementing the interrupt priority register 212 as a read/write register, the assigned priority values ***may be updated or changed under software control***." Ex. 5, 6:60-63. Likewise, another portion of the patent provides: "The context switch could be based on an OS context ID, power management modes, security modes, and other system defined modes where priority levels would differ." *Id.*, Abstract. In other words, the patent as a whole describes some embodiments in which updates may occur under software control, and other embodiments in which that does not occur. Conte ¶¶ 50-51. Against that background, it is unsurprising that the claim terms at issue are not restricted to one embodiment or the other; they are more general, so as to encompass both approaches described. Interpreting the claims in a manner that excludes the embodiment in bold italics above would be improper for this additional reason. *E.g.*, *C.R. Bard*, 388 F.3d at 865; *see also* Conte ¶ 51 ("a person of ordinary skill in the art would recognize that the patent described both approaches and included claims that encompassed both").

When Intel's proposal is considered in the context of the surrounding claim language, as it would need to be by the jury, the errors in Intel's interpretation become even more apparent. For example, Intel would have the Court edit claim 17 as follows:

> storing a plurality of ~~sets of priority levels in one or more storage devices~~ ***hardware for storing priority levels that are not rewritten by software when the system changes mode or context***, where each set of priority levels is associated with a different system mode and specifies a priority level for each potential pending interrupt request

As an initial matter, Intel omits the "one or more" language that appears in claim 17. It is improper to construe claims in a manner that omits their express limitations. *See Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 29 (1997) ("Each element contained in a patent claim is deemed material to defining the scope of the patented invention . . . ."). Intel seemingly seeks to replace "one or more" with "a plurality." But in patent claims, the term "plurality" means ***two*** or more, not one or more. *Dayco Prod., Inc. v. Total Containment, Inc.*, 258 F.3d 1317, 1327 (Fed. Cir. 2001). There is no basis for altering the claim in this manner.

That, however, is only the beginning of Intel's problems. Intel also seeks to add another entirely new element not required by any part of the claims: "***storing*** a plurality of ***hardware***." The claims require storing data in hardware, not storing the hardware itself, whatever that would mean. For example, the actual language of claim 17 calls for "storing a plurality of sets of priority levels in one or more storage devices." The specification is in accord, as it discloses "one or more storage devices are provided for storing a plurality of sets of priority levels . . . ." Ex. 5, 10:51-55. As noted above, VLSI does not object to providing that a storage device is hardware for storing information. But requiring, in addition, that the hardware for storing information must itself also be stored is another matter. That is not suggested in the claims or any other part of the patent. It is

not how a person of skill would understand the claims. And it would make no sense. This is an independent reason why Intel's attempt to rewrite the claims is fundamentally flawed.

The impropriety of Intel's proposals is further underscored by the fact that Intel is giving almost exactly the same meaning to two materially different terms, in violation of both common sense and law. The term "storage device for storing priority level information" in claims 1 and 9 is directed to storage devices, *e.g.*, hardware for storing information. In contrast, "sets of priority levels in … storage devices" in claim 17 is directed to priority levels, which may be stored in storage devices but are not themselves storage devices. Intel's suggestion that these disparate terms should be altered so that they both become directed to storage devices fails to give effect to their plainly different language. It is well-established that "the use of two terms in a claim requires that they connote different meanings." *Applied Med. Res. Corp. v. U.S. Surgical Corp.*, 448 F.3d 1324, 1333 n.3 (Fed. Cir. 2006); *see also CAE Screenplates Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000) ("In the absence of any evidence to the contrary, [the court] must presume that the use of these different terms in the claims connotes different meanings." This is yet another reason why Intel's proposed revisions to these terms should be rejected.

3. "providing a plurality of interrupt priority storage devices comprising a first interrupt priority storage device for storing priority level information associated with a first system mode, and a second interrupt priority storage device for storing priority level information associated with a second system mode; and providing a plurality of interrupt priority storage devices comprising a first interrupt priority storage device for storing priority level information associated with a first system mode for each of the one or more interrupt requests, and a second interrupt priority storage device for storing priority level information associated with a second system mode for each of the one or more interrupt requests"

VLSI's Proposal	Intel's Proposal
Definite	Indefinite

"[A] patent's claims, viewed in light of the specification and prosecution history, [must] inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014). Intel must prove indefiniteness by clear and convincing evidence. *BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1365 (Fed. Cir. 2017). Intel contends the below language renders claim 1 indefinite:

> [1] providing a plurality of interrupt priority storage devices comprising a first interrupt priority storage device for storing priority level information associated with a first system mode, and a second interrupt priority storage device for storing priority level information associated with a second system mode; and
>
> [2] providing a plurality of interrupt priority storage devices comprising a first interrupt priority storage device for storing priority level information associated with a first system mode ***for each of the one or more interrupt requests***, and a second interrupt priority storage device for storing priority level information associated with a second system mode ***for each of the one or more interrupt requests***;

The language in each element is identical, except for the bolded, italicized portions above. Intel incorrectly argues:

> A person of ordinary skill in the art would not understand whether the "a plurality of interrupt priority storage devices," "a first interrupt priority storage device," "a first system mode," "a second interrupt priority storage device," and "a second system mode" recited in (1) is the same as the "a plurality of interrupt priority storage devices," "a first interrupt priority storage device," "a first system mode," "a second interrupt priority storage device," and "a second system mode" recited in (2).

Ex. 10 (Intel's Preliminary Invalidity Contentions), 796-97. One skilled in the art would understand that the overlapping, identically phrased portions of the two elements could be satisfied by the same structures. Conte ¶ 56. There is nothing to suggest that different structures are required. *Id.* A structure that satisfied the language the first time it appears would, by definition, satisfy the same language the second time as well. Of course, to satisfy the second element that

structure must also satisfy the bolded, italicized language above, which is not required in the first element. *Id.* ¶ 59. In other words, taken as a whole the two elements are not redundant.[4] *Id.*

Where the inventors wanted to require two different structures, they stated so explicitly. For example, where they wanted to require two different interrupt storage devices, they called for a "first interrupt priority storage device" and a "second interrupt priority storage device." And where they did not want to require two different structures, they did not do so.

The specification is consistent with both claim elements being satisfied by a single structure. *Id.* ¶ 58. For example, the patent discloses:

> At step 403, a plurality of interrupt priority storage devices (e.g., interrupt priority registers) are provided, including a first interrupt priority storage device for storing priority level information (e.g., a first multi-bit priority level indication) associated with a first system mode, and a second interrupt priority storage device for storing different priority level information (e.g., a second multi-bit priority level indication) associated with a second system mode, where each multi-bit priority level indication is assigned to a corresponding interrupt signal.

Ex. 5, 9:24-33. That is, the limitations identified by Intel ("a plurality of interrupt priority storage devices," "a first interrupt priority storage device," "a first system mode," "a second interrupt priority storage device," and "a second system mode") are discussed in the context of a "multi-bit priority level indication . . . assigned to a corresponding interrupt signal." There is no indication in the specification that the relevant limitations are separate and apart from priority level information "for each of the one or more interrupt requests."

There is nothing inherently wrong with the patent's description or claims. It is well-settled that the same component of an accused device can satisfy multiple claim limitations. For example,

[4] Even if the two elements were redundant, that would not render the claim indefinite. *See, e.g.*, *Team Worldwide Corp. v. Wal-Mart Stores, Inc.*, 2018 WL 1353116, at *12 & n.13 (E.D. Tex. Mar. 15, 2018) (holding "The [c]ourt disagrees that redundancy of limitations in a claim necessarily renders the claim invalid" and discussing authorities).

in *Powell*, 663 F.3d at 1231-32, the Federal Circuit found that the claimed "cutting box" and "dust collection structure" element need not be separate components for purposes of the infringement analysis, because the specification supported a broader view under which they could be the same component. Similarly, in *Linear Technology Corp. v. Int'l Trade Comm'n*, 566 F.3d 1049, 1055 (Fed. Cir. 2009), the Federal Circuit held that the claimed "second circuit" and "third circuit" did "not require entirely separate and distinct circuits," because "nothing in the claim language or specification that supports narrowly construing the terms to require a specific structural requirement or entirely distinct 'second' and 'third' circuits." These elements are not indefinite by any measure, and certainly not by clear and convincing evidence.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

A true and correct copy of the foregoing instrument was served or delivered electronically via U.S. District Court [LIVE] — Document Filing System, to all counsel of record, on this 30th day of October, 2019.

/s/ J. Mark Mann
J. Mark Mann